TRIMON CT250

Feature Specification

- High-Performance Cached Multi-Threaded MIPS I Instruction Set Compatible Processor Core

- Extensions and accelerators to the Instruction Set can be added

- Hardware multi-threaded support

- 4 hardware threads supported (scalable to 8, 16, 32)

- Dedicated program context storage

- Single cycle thread swap

- Configurable Register Files Alocation to Running Instruction Therads

- Two Staged Fully Pipelined Instruction Cache. The associativity and size of Instruction Cache are configurable based on application requirements.

- Two Staged Fully Pipelined Data Cache. The associativity and size of Data Cache are configurable based on application requirements.

- 250MHz Operating frequency in 0.18um TSMC process

- Operating frequency can be increased if necessary.

- 0.3mm**2 in 0.18 TSMC process without memories

- 1.5mm**2 in 0.18 TSMC process including memories

- Support for 3 external indepenedent memory systems, memory load-store units included.

- The External Memory Interface is scalable and it can support different partitioning.

- Gaskets can be added to support buses like AMBA etc.

- RS232 based software debugger (optional)

- Ideal for SoC data-communication, packet processors, packet classification engines and embedded applications.

The TRIMON CT250 IP Package

- TRIMON CT250 Verilog RTL

- Verilog Testbench

- Verification Environemnt, scripts and tools

- Assembler development toolchain

- "C" development toolchain

- Micro-Kernel program management firmware

Block Diagram