



CACHE CONTROLLER

Multi-purpose Cache controller

Feature Specification

- Direct-Mapped, Set-Associative And Associative Cache Compatible
- Configurable For Any Number Of Words Per Cache-Lines
- Configurable For Any Number Of Cache Memory Banks
- Configurable For 8, 16, 32, 64-bit Data Width
- Configurable For Any Number Of Cache Lines
- AMBA AXI Memory Interface Support
- Other Interface Protocols Support Can Be Added If Needed
- Performance Optimization Features:
 - Critical Word First Fetch Capability
 - Cache-line Fetch Support With Address Wrap-Around Capability
 - Write-back Buffer For Cache-Line Write-Back Optimization

The CACHE CONTROLLER IP Package

- Cache Controller Verilog RTL
- Verilog Testbench
- Verification Environment, scripts and tools
- Configurable Test Transaction Toolchain
- Synthesis And STA Scripts
- Documentation

Block Diagram

