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Direct-Mapped CACHE

High-performance Direct-Mapped Cache System

Feature Specification

- Configurable Cache Line support for 4, 8, 16, 32 Word Cache-Lines
- Configurable Data Width supportf for 8, 16, 32, 64-bit Data Width
- Configurable number of Cache Lines - 32, 64, 128,, 256, 512, 1024, 2048 Cache Lines supported
- Two-staged Fully Pipelined architecture
- AMBA AXI Memory Interface Support
- Stall And Flush Control Enabled
- Performance Optimization Features:
- Critical Word First Fetch Capability
- Cache-line Fetch Support With Address Wrap-around Capability
- Write-back Buffer For cache-line write-back optimization
- Suitable For Both Instruction And Data Memory Caches.

The CACHE SYSTEM IP Package

- Cache System Verilog RTL
- Verilog Testbench And Tests
- Verification Environemnt, Scripts And Tools
- Configurable Test Transaction Toolchain
- Synthesis And STA Scripts
- Documentation

Block Diagram