FUNCTIONAL VERIFICATION DESIGN FLOW SPECIFICATION ARCHITECTURE RTL DESIGN FUNCTIONAL DYNAMIC DESIGN VERIFICATION SYNTHESIS POST SYNTHESIS STATIC TIMING ANALYSIS FUNCTIONAL STATIC DESIGN VERIFICATION PASS YES NO PASS YES ALL LAYOUT POST LAYOUT STATIC TIMING ANALYSIS POST LAYOUT DESIGN VERIFICATION NO PASS PASS YES YES ALL LVS/DRC/ANTENA OTHERS

NO

PASS

YES

TAPEOUT