



## SDRAM Controller

High-Performance Universal SDRAM Memory Controller Core

### Feature Specification

- Support of AMBA AXI and AMBA AHB interfaces
- Read and write FIFOs with configurable length
- Configurable master system and memory bus width
- Reordering function for maximum bandwidth
- Fully programmable SDRAM parameters
- Dynamically reconfigurable memory burst length
- Fully software based memory initialization and configuration
- Built in self test
- ECC - optional
- Mobile low power applications functionality

### The SDRAM Controller IP Package

- SDRAM Controller Verilog RTL and Netlist
- Full controller specification
- Verilog Testbench
- Test plan documentation
- Verification Environment, scripts and tools
- Primetime timing scripts
- Synopsys synthesis scripts

### Block Diagram

#### SIBIZ SDRAM Controller

